

60A, 30V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 60A, 30V
- $r_{DS(ON)} = 0.027\Omega$
- Temperature Compensating PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG60P03, RFP60P03, RF1S60P03 and RF1S60P03SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

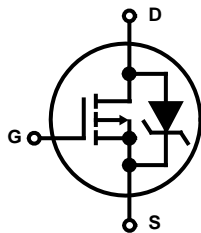
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG60P03	TO-247	RFG60P03
RFP60P03	TO-220AB	RFP60P03
RF1S60P03	TO-262AA	F1S60P03
RF1S60P03SM	TO-263AB	F1S60P03

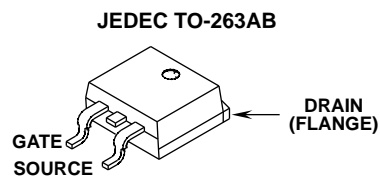
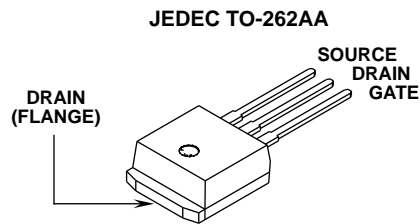
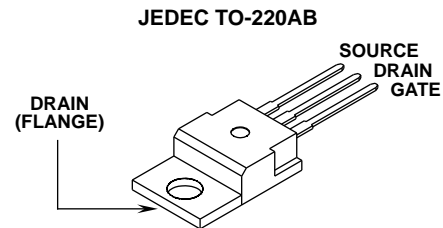
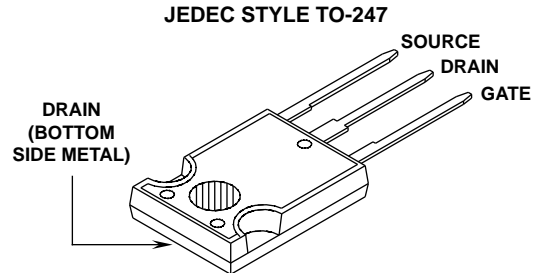
NOTE: When ordering use the entire part number.

Formerly developmental type TA49045.

Symbol



Packages



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

		RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM	UNITS
Drain Source Voltage	V_{DSS}	-30	V
Drain Gate Voltage	V_{DGR}	-30	V
Gate Source Voltage	V_{GS}	± 20	V
Drain Current			
RMS Continuous	I_D	60	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^\circ\text{C}$	P_D	176	W
Derate above +25°C	P_T	1.17	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Specifications RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	-30	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	-2	-	-4	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{V}$, $V_{GS} = 0\text{V}$	$T_C = +25^\circ\text{C}$	-	-	-1	μA
			$T_C = +150^\circ\text{C}$	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
On Resistance	$r_{DS(ON)}$	$I_D = 60\text{A}$, $V_{GS} = -10\text{V}$	-	-	0.027	Ω	
Turn-On Time	t_{ON}	$V_{DD} = -15\text{V}$, $I_D = 60\text{A}$ $R_L = 0.25\Omega$, $V_{GS} = -10\text{V}$ $R_{GS} = 2.5\Omega$	-	-	140	ns	
Turn-On Delay Time	$t_{D(ON)}$		-	20	-	ns	
Rise Time	t_R		-	75	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	35	-	ns	
Fall Time	t_F		-	40	-	ns	
Turn-Off Time	t_{OFF}		-	-	115	ns	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 0$ to -20V	$V_{DD} = -24\text{V}$, $I_D = 60\text{A}$, $R_L = 0.4\Omega$	-	190	230
Gate Charge at 10V	$Q_{G(-10)}$	$V_{GS} = 0$ to -10V	-		100	120	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to -2V	-		7.5	9	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	3000	-	pF	
Output Capacitance	C_{OSS}		-	1500	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	525	-	pF	
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	0.85	$^\circ\text{C/W}$	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	-	-	80	$^\circ\text{C/W}$		

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -60\text{A}$	-	-	-1.75	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -60\text{A}$, $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	200	ns

Typical Performance Curves

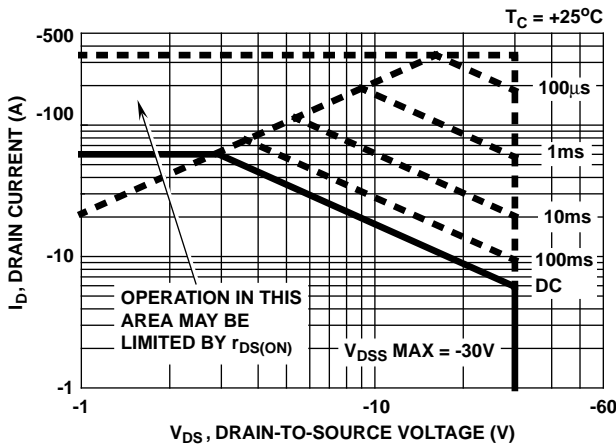


FIGURE 1. SAFE OPERATING AREA CURVE

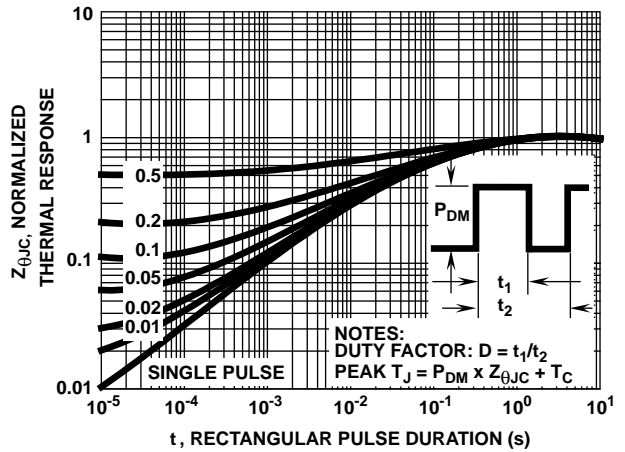


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

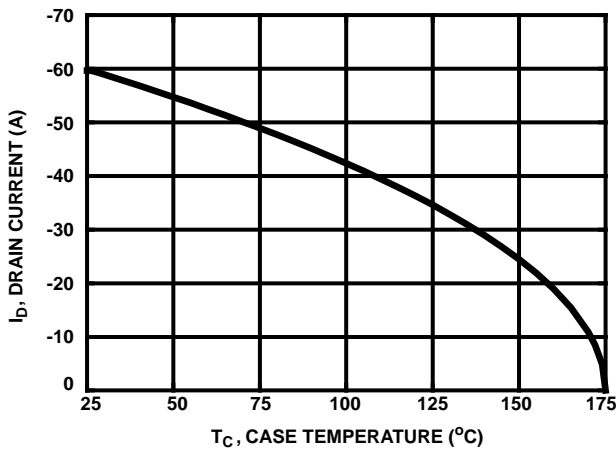


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

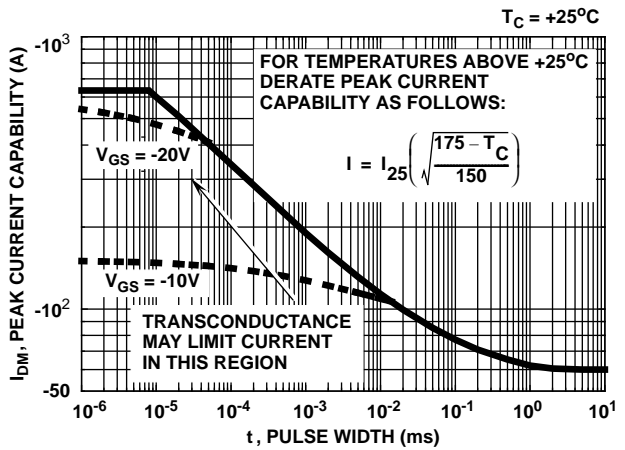


FIGURE 4. PEAK CURRENT CAPABILITY

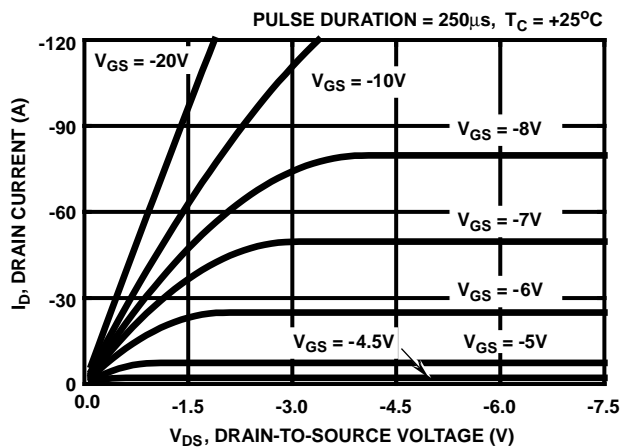


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

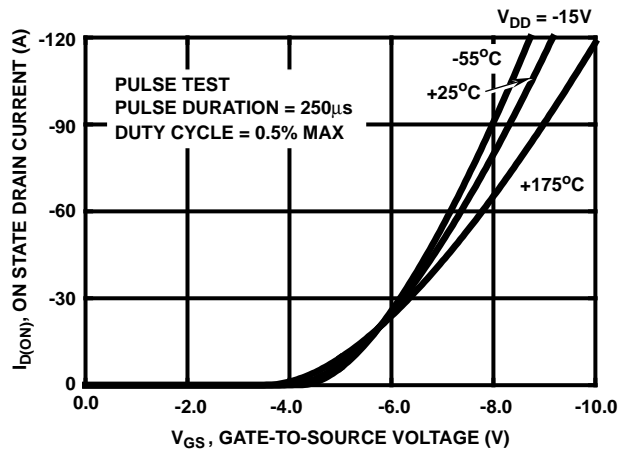


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

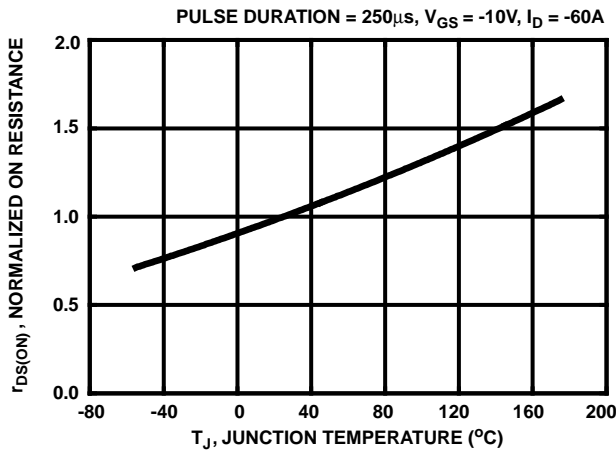


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

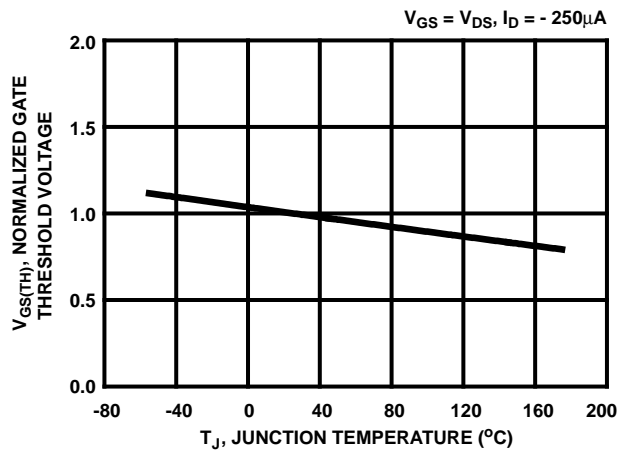


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

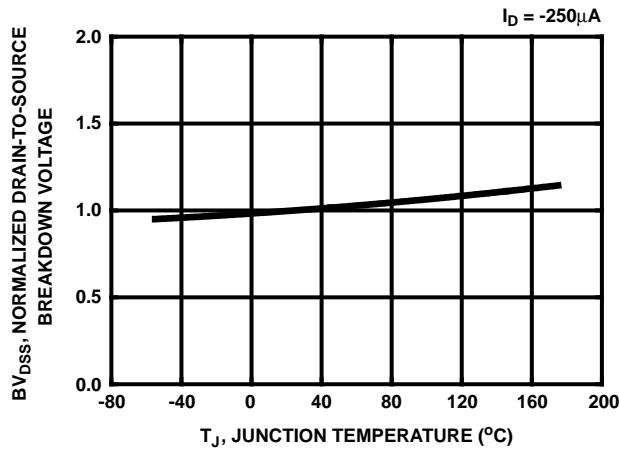


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

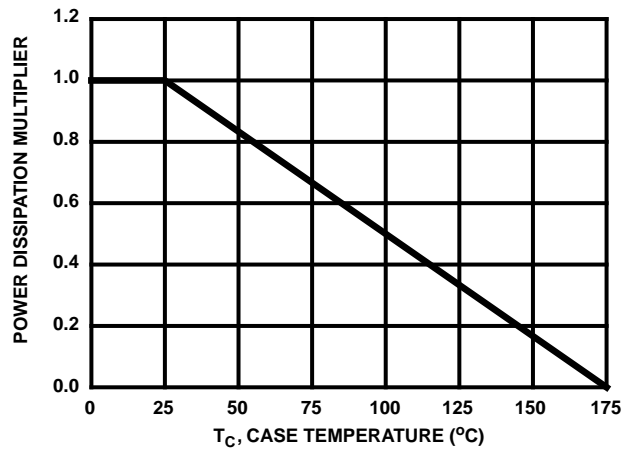


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS

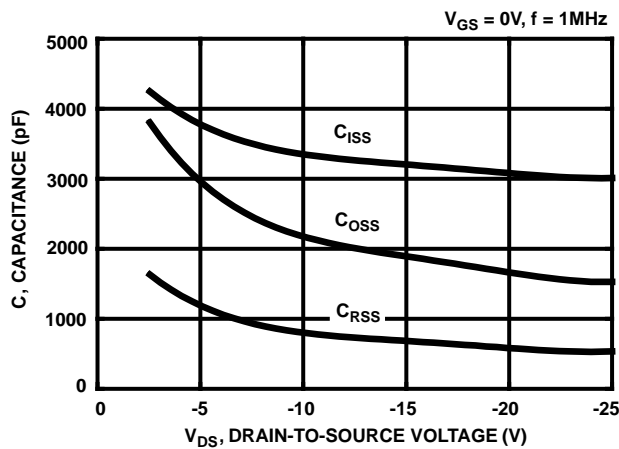


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

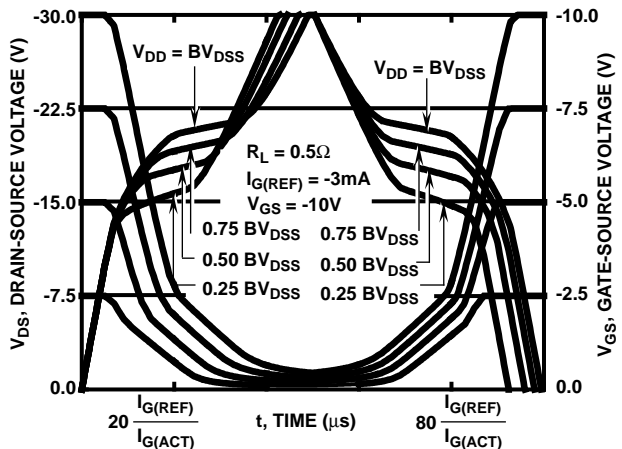


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

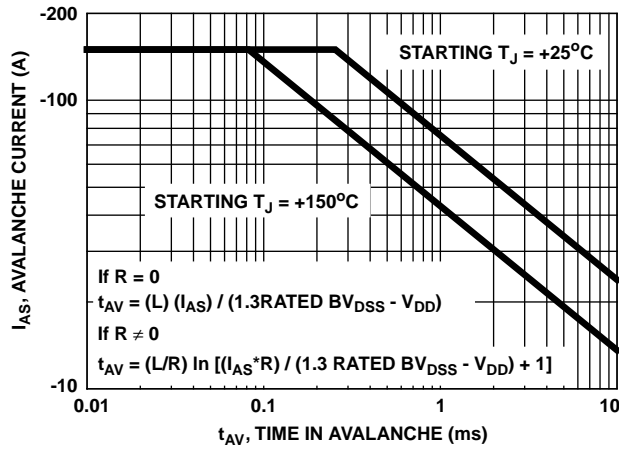


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

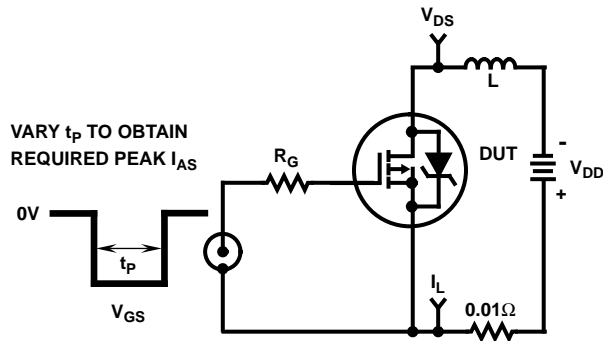


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

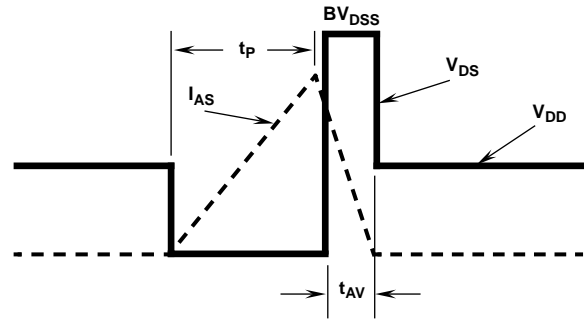


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

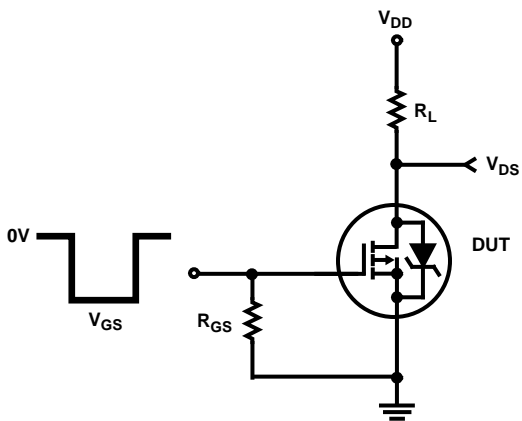


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

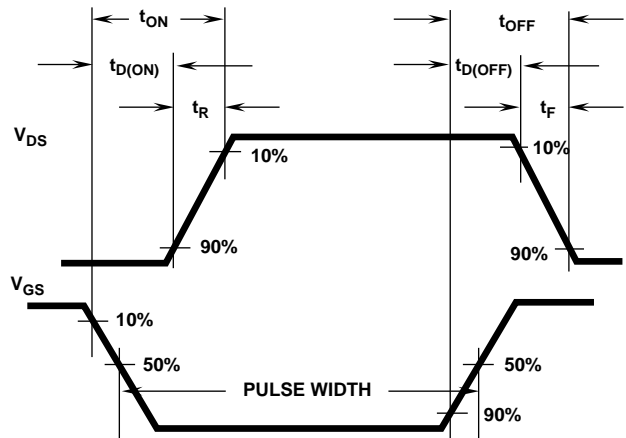


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

